REMARKS

Claims 1, 3-5, 8, and 10-13 are now pending in the application. By this paper, Claims 1 and 11-13 have been amended. The basis for these amendments can be found throughout the specification, claims, and drawings originally filed. No new matter has been added. The preceding amendments and the following remarks are believed to be fully responsive to the outstanding Office Action and are believed to place the application in condition for allowance.

The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 3-5, 8, 10, 11, and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nishimura et al. (U.S. Patent No. 6,781,241).

This rejection is respectfully traversed.

Independent Claim 1 calls for a semiconductor device having a first semiconductor chip mounted on a first carrier substrate. A second carrier substrate is connected to the first carrier substrate by protruding electrodes, which cause the second carrier substrate to be held above and spaced apart from the first semiconductor chip such that a gap is created between the second carrier substrate and the first semiconductor chip. Similarly, independent Claim 13 calls for an electronic device including a first electronic part mounted on a first carrier substrate. A second carrier substrate is connected to the first carrier substrate by protruding electrodes, which cause the second carrier substrate to be held above and spaced apart from the

first electronic part such that a gap is created between the second carrier substrate and the first electronic part.

Independent Claim 11 calls for an electronic device including a first semiconductor chip mounted on a first carrier substrate. A second carrier substrate having a third semiconductor chip mounted thereon is bonded to the first carrier substrate by protruding electrodes. A gap is created between a bottom surface of the second carrier substrate opposite the third semiconductor chip and a top surface of the first semiconductor chip such that the second carrier substrate is spaced apart from the first semiconductor chip.

In this manner, the present invention calls for a first semiconductor chip or electronic part to be mounted to a first carrier substrate and a second carrier substrate connected to the first carrier substrate such that the second carrier substrate is spaced apart from the first semiconductor chip or first electronic part mounted on the first carrier substrate. Because the second carrier substrate is spaced apart from the first semiconductor chip or first electronic part, a gap is created between the second carrier substrate and the first semiconductor chip or first electronic part.

Nishimura fails to teach a second carrier substrate spaced apart from a first semiconductor chip or first electronic part mounted on a first carrier substrate such that a gap is created between the second carrier substrate and the first semiconductor chip or first electronic part. Rather, Nishimura teaches a stacked-type semiconductor device including a first carrier substrate (1b) having a first semiconductor chip (3b) disposed on a top surface thereof and a second semiconductor chip (3f) disposed on a bottom surface thereof generally opposite from the top surface. See Nishimura at Column 5,

lines 12-24 and Figure 6. Nishimura also teaches a second carrier substrate (1a) having a plurality of stacked semiconductor chips positioned thereon (3c), (3d). See Nishimura at Figure 6. The second carrier substrate is positioned generally above the first carrier substrate and is bonded thereto by a series of solder balls (7). However, the first semiconductor chip (3b) is in contact with the second carrier substrate (1a) by an adhesive (9). See Nishimura at Column 5, lines 18-21 and Figure 6. Because the adhesive (9) connects the first semiconductor chip (3b) to the second carrier substrate (1a), Nishimura fails to teach separating a second carrier substrate from a first semiconductor chip mounted on a first carrier substrate such that a gap is created between the second carrier substrate and the first semiconductor chip. Therefore, Nishimura fails to teach each and every element of the claimed invention.

Because Nishimura fails to teach a second carrier substrate spaced apart from a first semiconductor chip or first electronic part mounted on a first carrier substrate such that a gap is created between the second carrier substrate and the first semiconductor chip or first electronic part, Applicant respectfully submits that Nishimura fails to teach each and every element of the present invention. Accordingly, Applicant respectfully submits that independent Claims 1, 11, and 13, as well as Claims 3-5, 8, and 10, respectively dependent therefrom, are in condition for allowance. Therefore, reconsideration and withdrawal of the rejection is respectfully requested.

Claim 12 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Degani et al. (U.S. PG Pub#20020079568).

This rejection is respectfully traversed.

Independent Claim 12 calls for a semiconductor device including a first semiconductor chip mounted on a carrier substrate. A third semiconductor chip is connected to the carrier substrate by protruding electrodes, which cause the third semiconductor chip to be held above and spaced apart from the first semiconductor chip such that a gap is created between the third semiconductor chip and the first semiconductor chip.

In this manner, the present invention calls for a semiconductor device having a first semiconductor chip mounted to a carrier substrate. A third semiconductor chip is mounted generally above the carrier substrate by protruding electrodes such that the third semiconductor chip is spaced apart from the first semiconductor chip mounted on the carrier substrate. Because the third semiconductor chip is spaced apart from the first semiconductor chip, a gap is created between the third semiconductor chip and the first semiconductor.

Degani fails to teach a third semiconductor chip held above and spaced apart from a first semiconductor chip mounted on a carrier substrate such that a gap is created between the third semiconductor chip and the first semiconductor chip. Rather, Degani teaches a stacked multi-chip module having an IC chip (107) mounted thereon. See Degani at pg. 4, Paragraph 62 and Figure 8. A substrate (106) is disposed above the IC chip (107) and is attached thereto by solder bumps (32). See Degani at pg. 4, Paragraph 62 and Figure 8. An IC chip (109) is attached to the substrate (106) such that the IC chip (109) is held above the IC chip (107) disposed on the motherboard (73). See Degani at fig. 8. While the IC chip (109) of the substrate (106) is generally held above the IC chip (107) of the motherboard (73); the IC chip (109) is not spaced apart

from the IC chip (107) as the IC chip (109) is attached to the IC chip (107) via solder balls (32) and substrate (106). See Degani at Figure 8. Because the IC chip (109) of the substrate (106) is attached to the IC chip (107) of the motherboard (73) a gap cannot be formed generally between the IC chip (109) and the IC chip (107).

Because Degani fails to teach a third semiconductor chip held above and spaced apart from a first semiconductor chip mounted to a carrier substrate such that a gap is created between the third semiconductor chip and the first semiconductor chip, Applicant respectfully submits that Degani fails to teach each and every element of the present invention. Accordingly, Applicant respectfully submits that independent Claim 12 is in condition for allowance. Therefore, reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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